

Revision : 1.0

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	APU DDRIII, PCI_E
05	APU CONTROL
06	APU POWER & GND
07	DDRIII CHANNEL A
08	HUDSON PCIE/PCI/CPU/LPC/CLK
09	HUDSON ACPI/GPIO/USB/AUDIO
10	HUDSON SATA/IDE/HWM/SPI
11	HUDSON POWER & GND
12	PCI, VGA
13	ITE 8728 EX
14	ALC887-VD2 CODEC
15	LPT ,COM ,F_USB ,FAN ,USB_HDMI
16	ATX, F_PANEL, PWR SEQ
17	VCORE (PWM RT8871)
18	SB, APU18 V, APU10V, VCC11_DUAL POWER
19	DDR POWER , VCC18
20	LAN RTL8111F

Model Name:GA-E240N

Component value change history

Version: 1.0

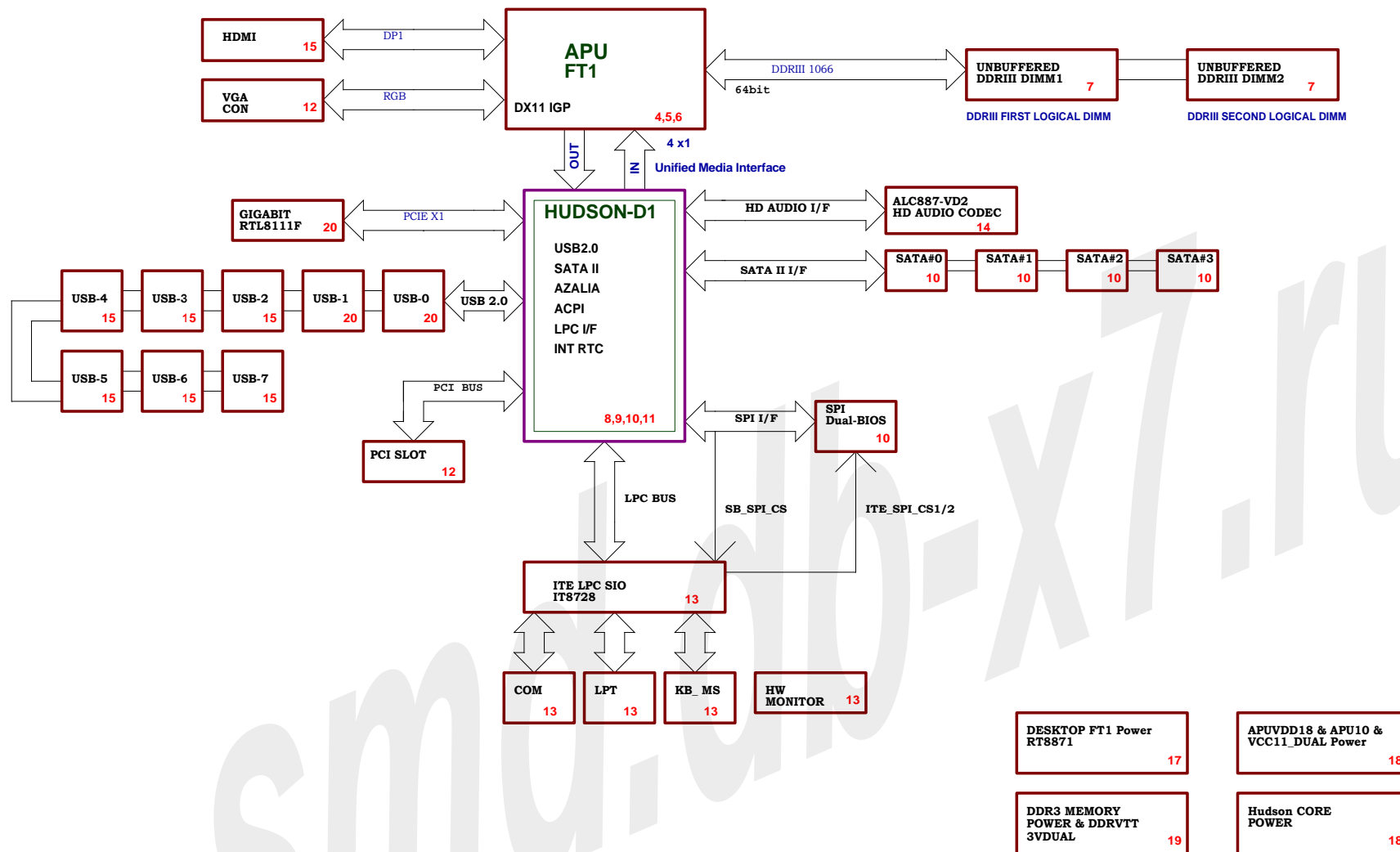
P-Code: U99054-0

[illegible]

Circuit or PCB layout change for next version

[illegible]

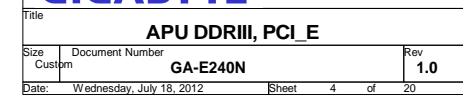
FT1 CUSTOMER DESKTOP REFERENCE DESIGN



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Title **BLOCK DIAGRAM**

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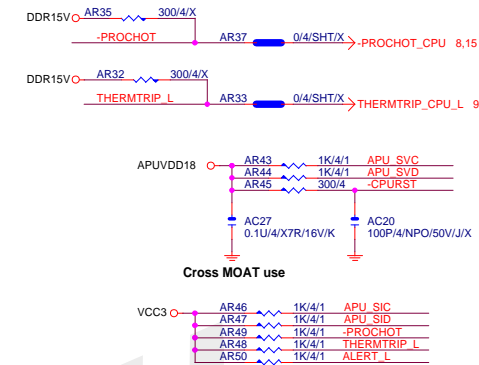
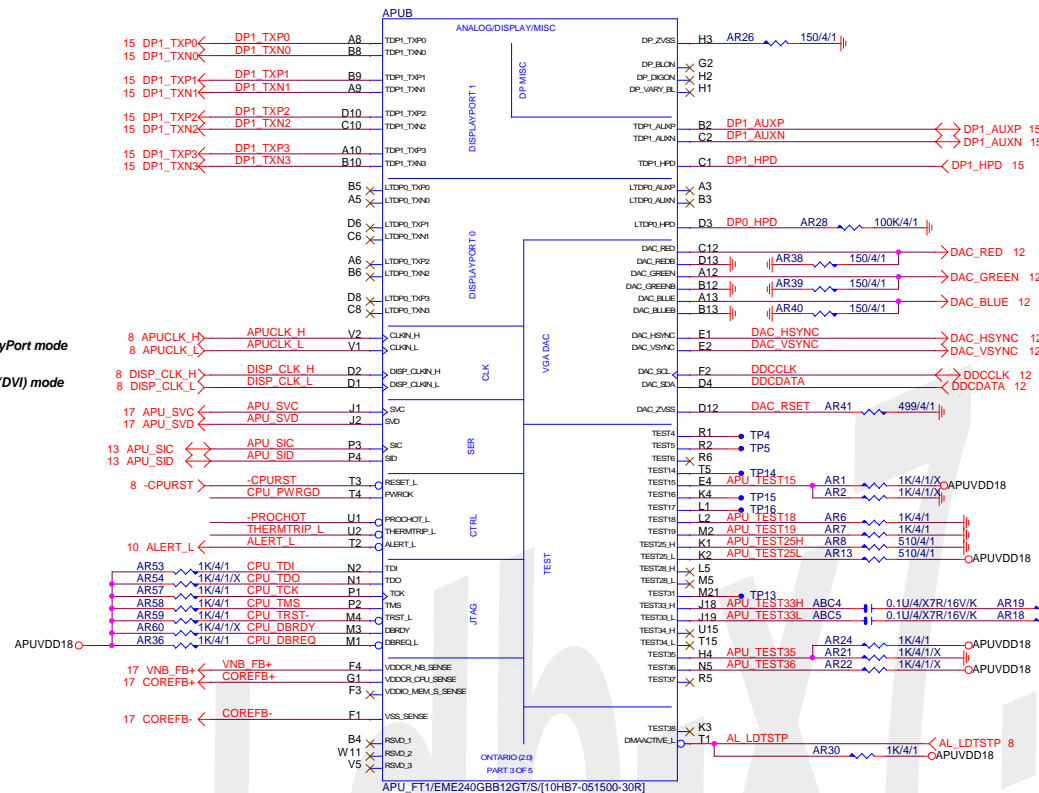
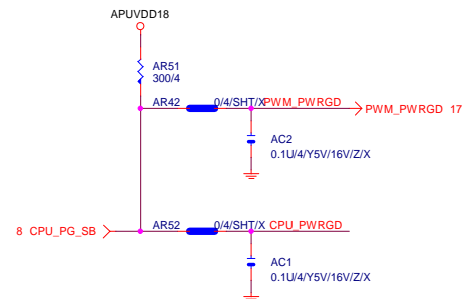


APU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 APU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
 VLDT_B = HT12B

Input clock for DisplayPort mode

Input clock for TMDS (DVI) mode

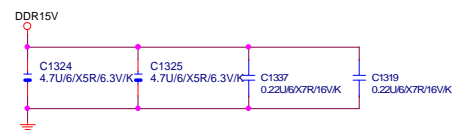
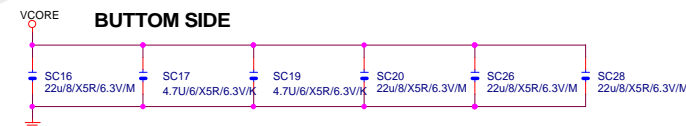
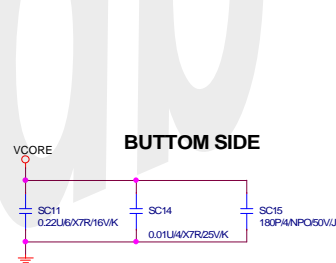
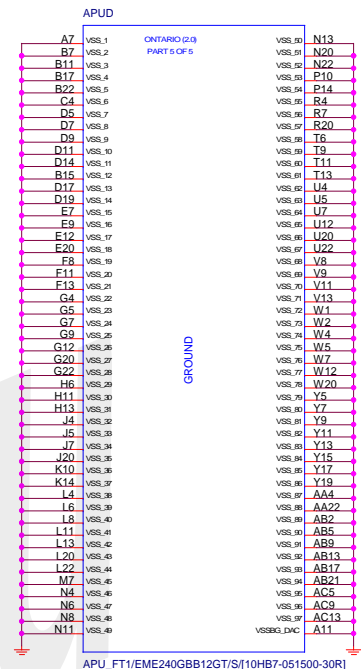


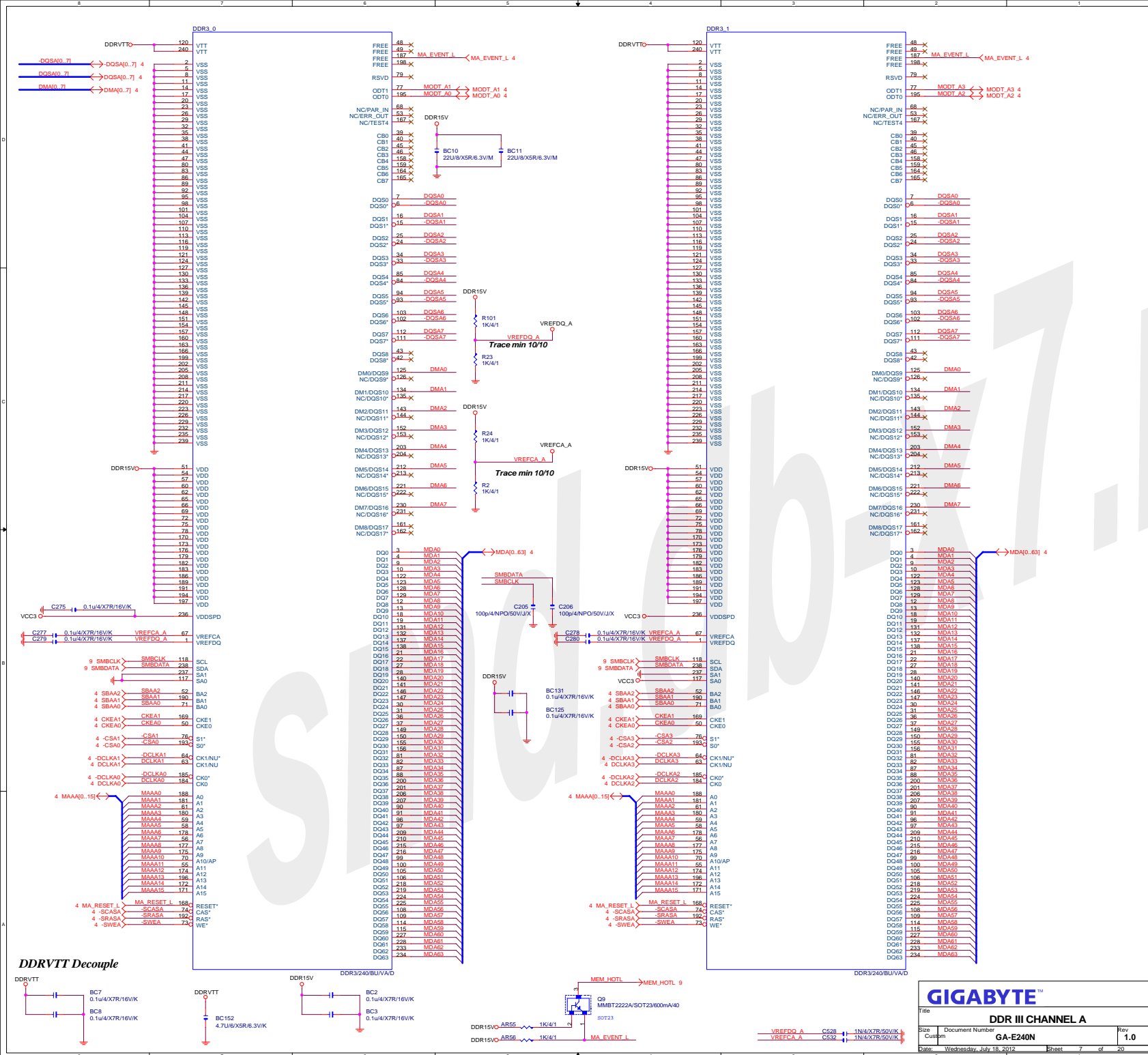
Cross MOAT use

TEST35: high=>HDMI enable,
low=>HDMI disable.

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Title			
APU CONTROL			
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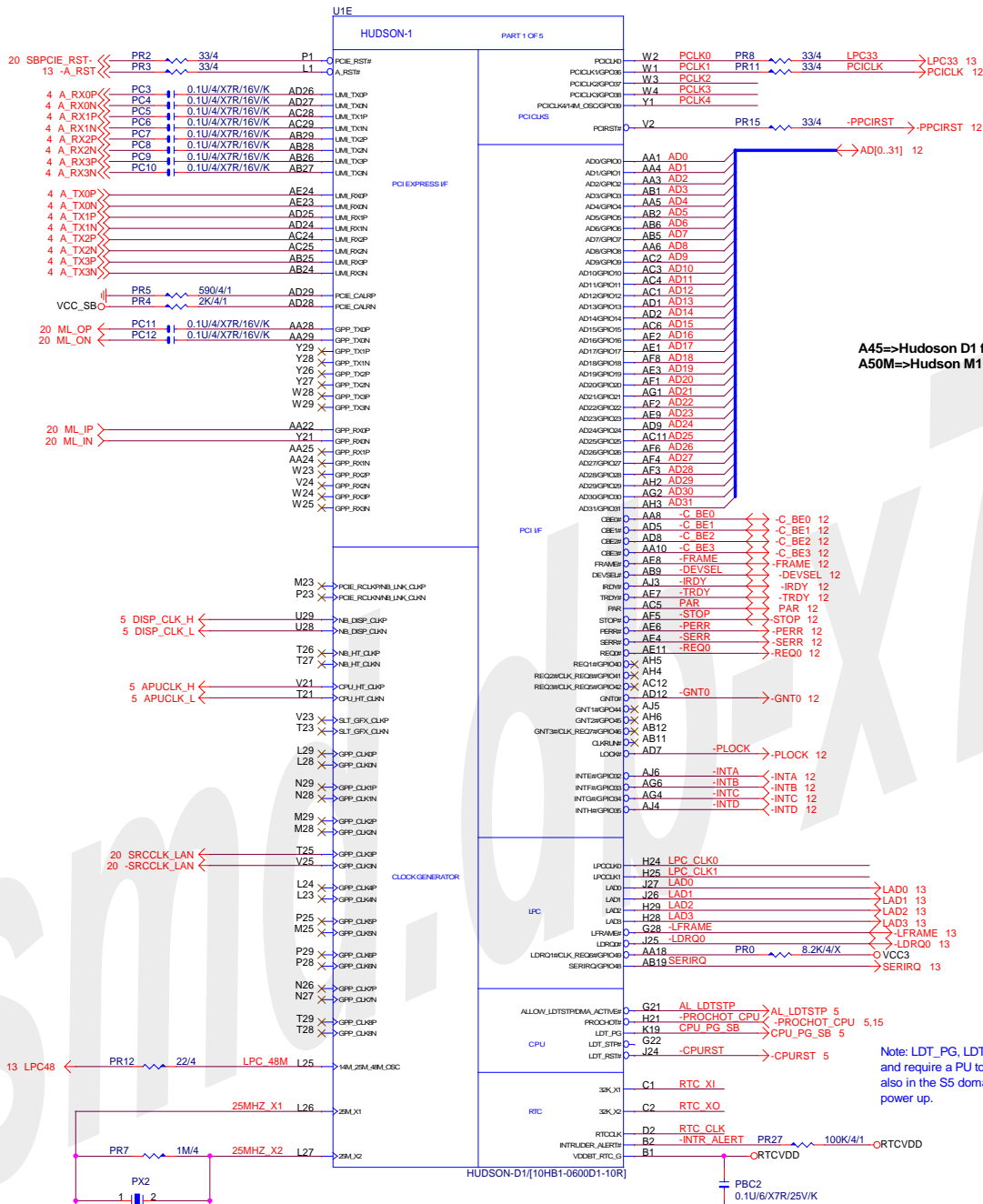






1 SB_HS

SB_HS/[12SP2-SA0301-01R_12SP2-SA0301-02R_12SP2-SA0301-03R]



A45=>Hudson D1 for Desktop,
A50M=>Hudson M1 for Mobile.

PCLK1 PR14 8.2K/4

Low: Force PCIE GEN1, High: Allow PCIE GEN2

Watch Dog Timer :Low=>Disable, High=>Enable

Debug Straps:Low=>Disable, High=>Enable

Fusion clock mode :Low=>Enable, High=>Disable

This strap is not used if the strap CLKGEN is configured for external clock generator mode.

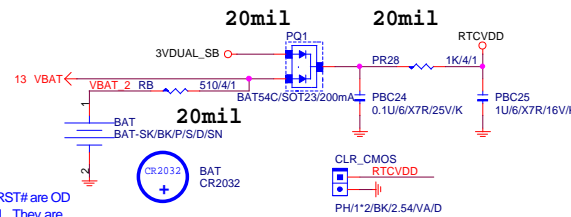
PEMC1 for EMI

LPC_CLK0 PR20 8.2K/4

3VDUAL_SMI
0

LPC_CLK0 LPC_CLK1

PULL HIGH	IMC ENABLED	Internal Clock Mode DEFAULT
PULL LOW	IMC DISABLED	External Clock Mode



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

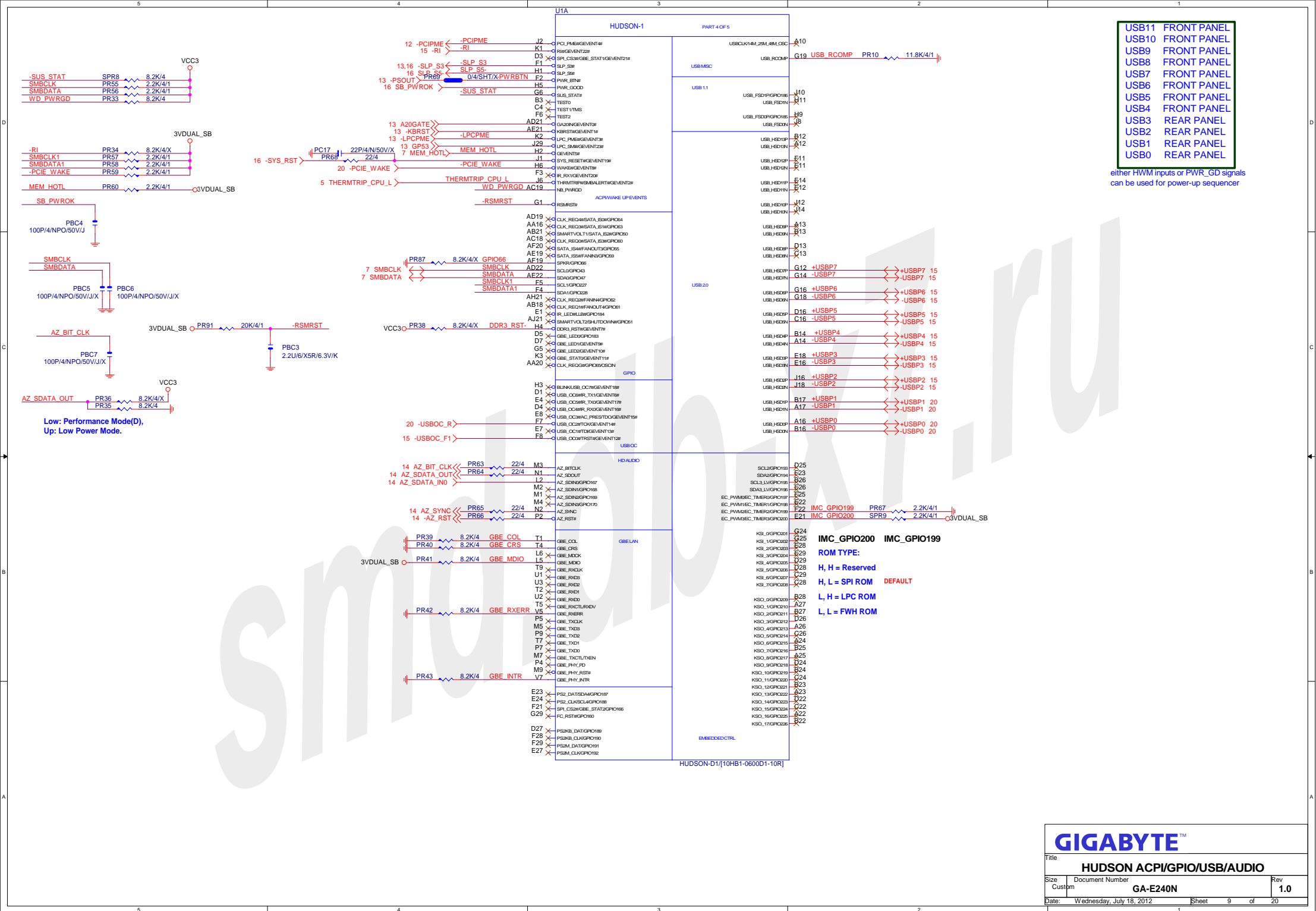
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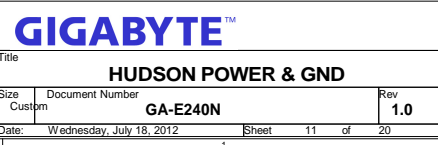
NOT ADD ICT FOR RTCVDD PIN

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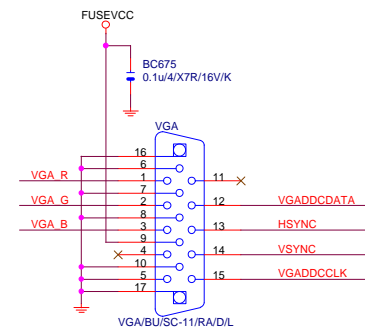
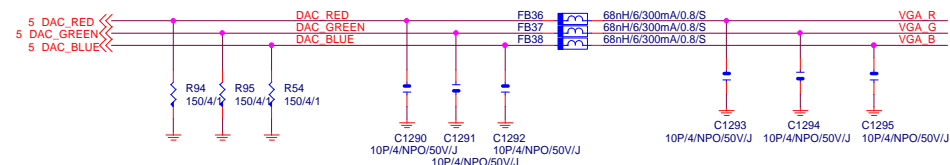
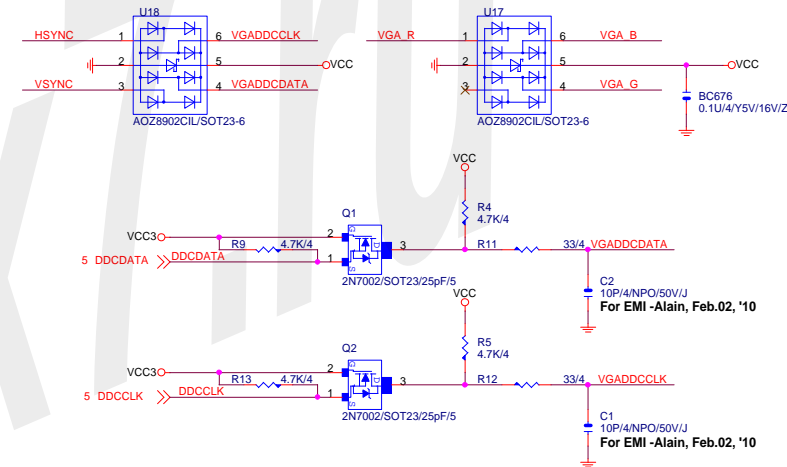
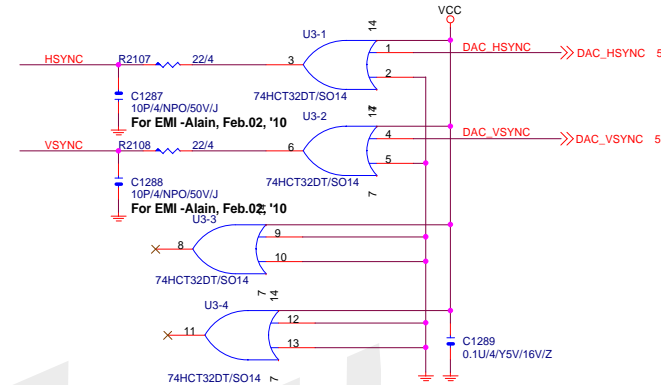
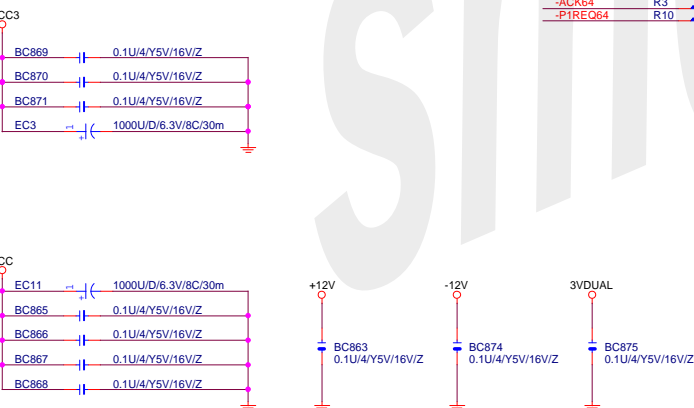
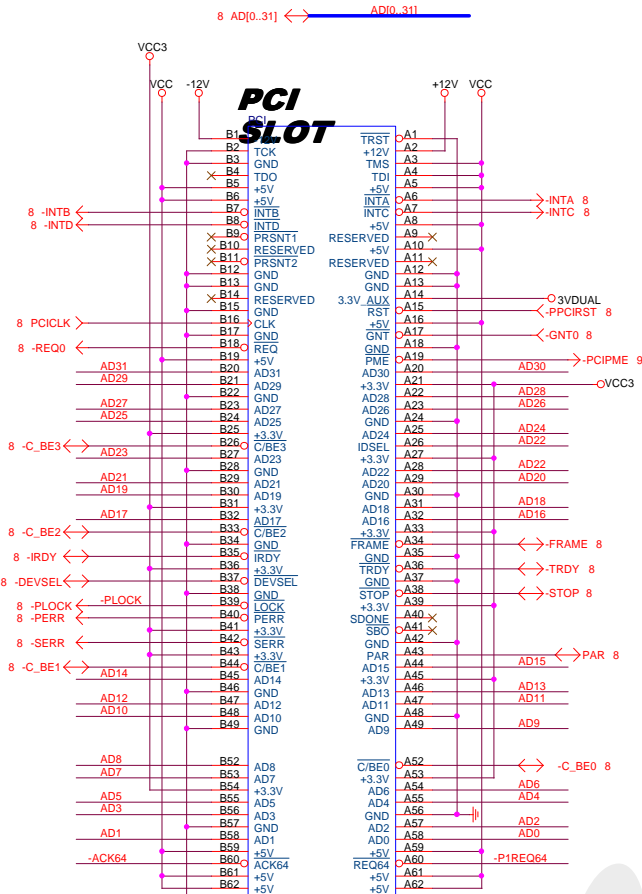
Title	HUDSON PCIE/PCI/CPU/LPC/CLK
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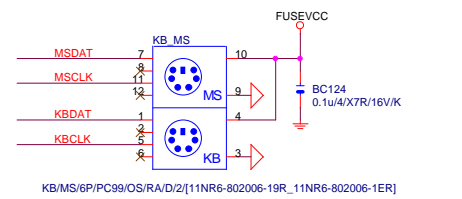
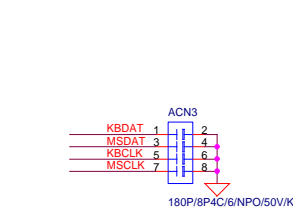
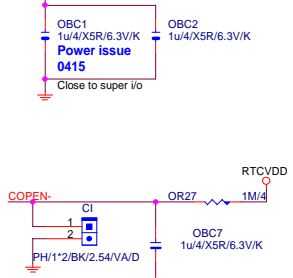
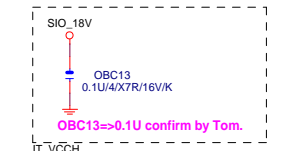
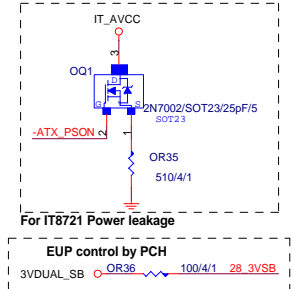
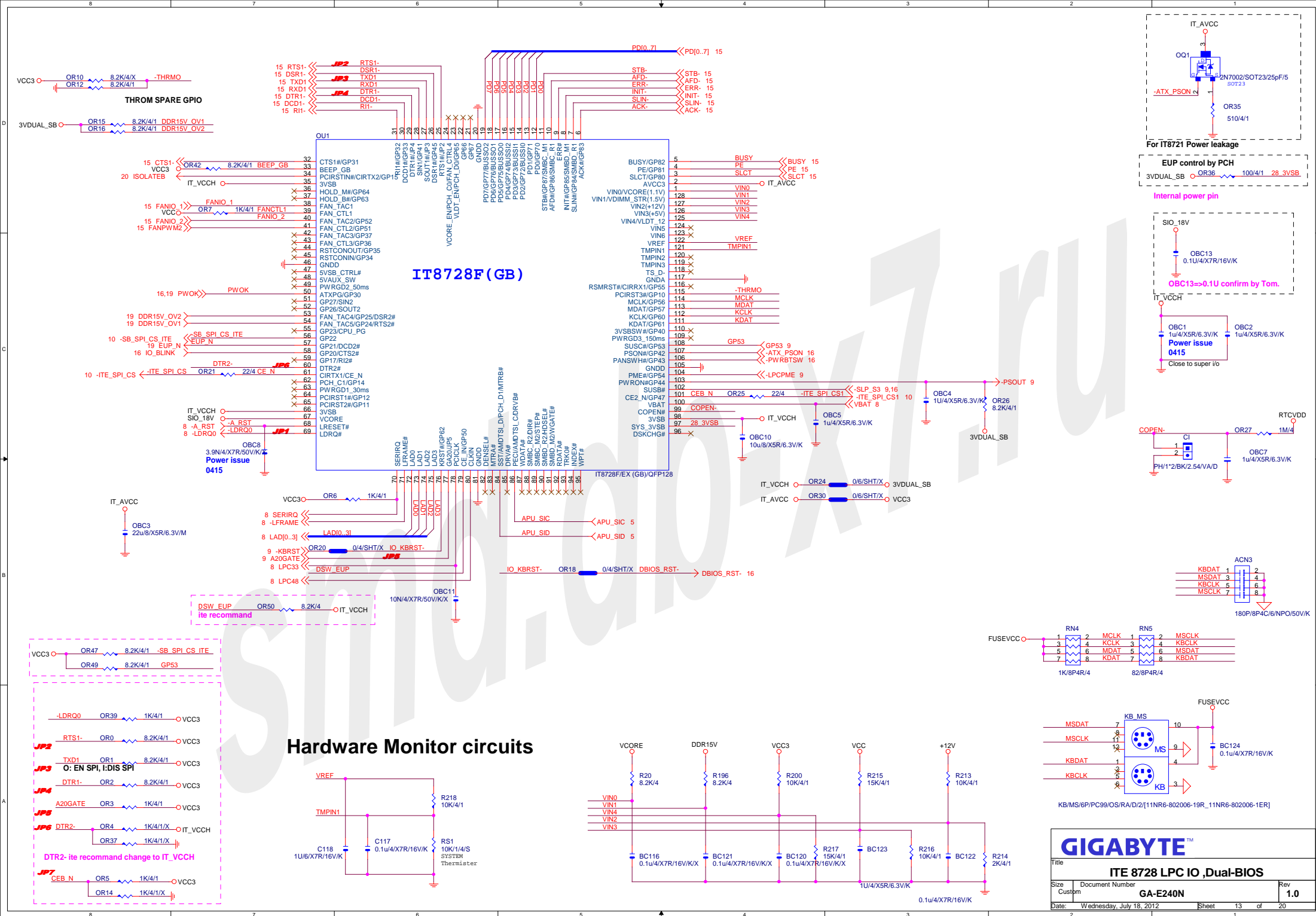




PCI SLOT



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PCI, VGA		
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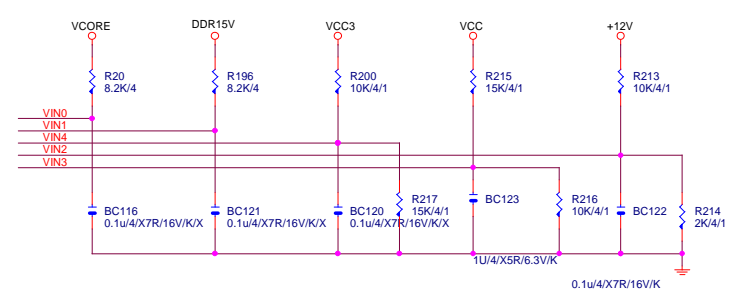
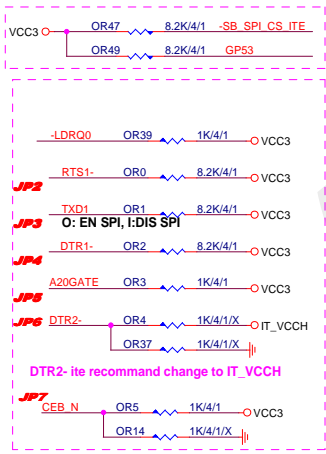
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ITE 8728 LPC IO ,Dual-BIOS

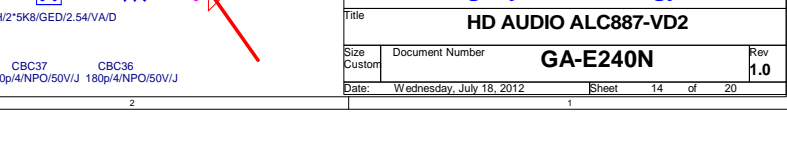
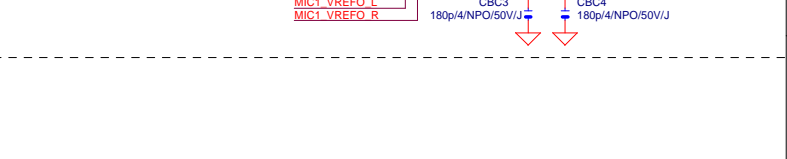
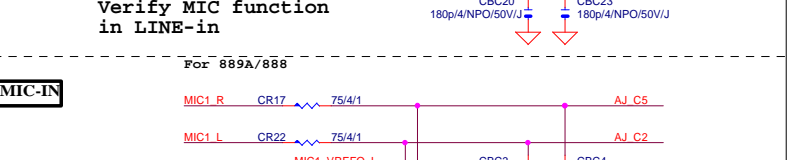
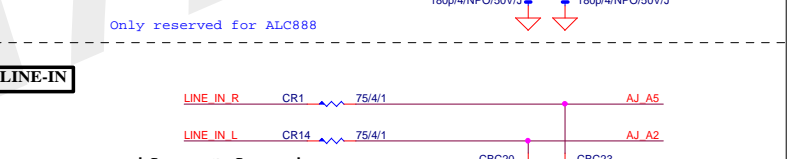
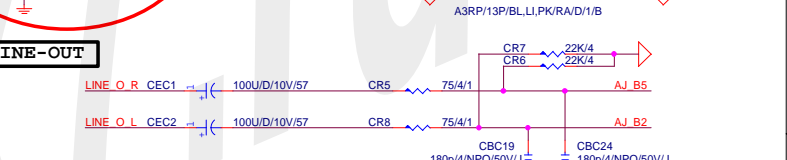
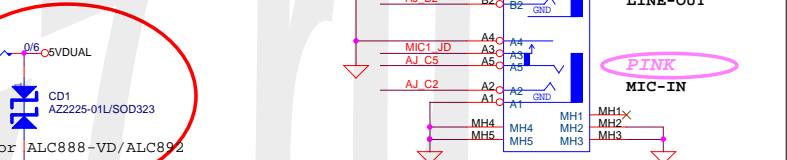
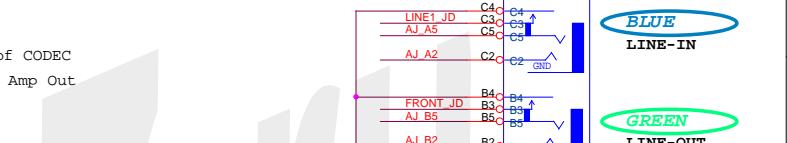
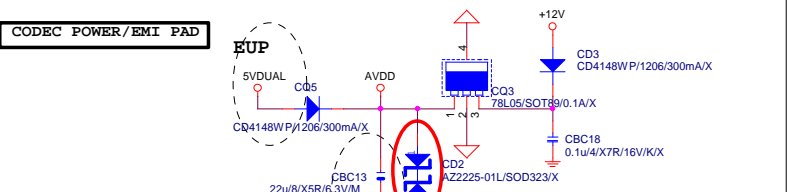
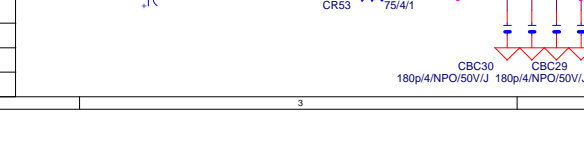
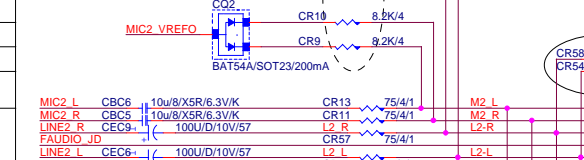
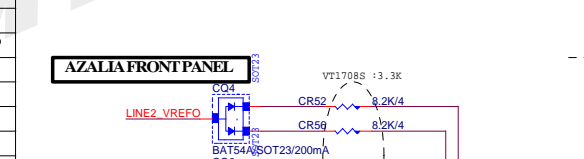
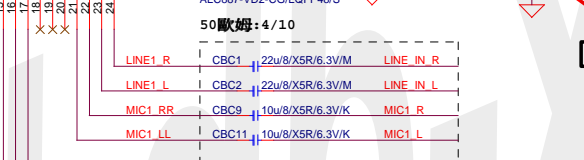
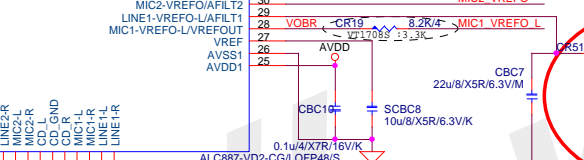
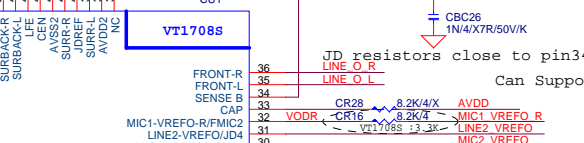
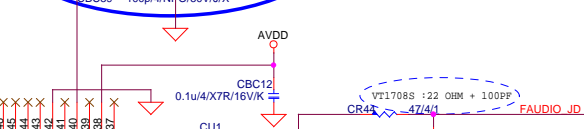
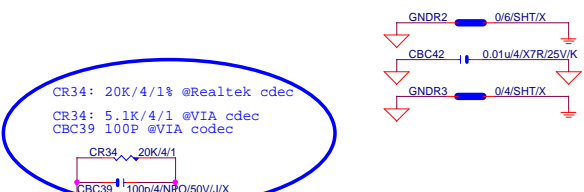
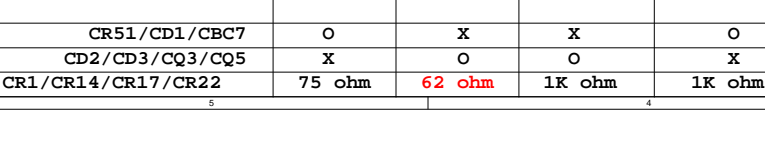
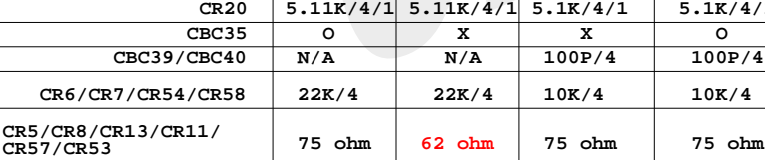
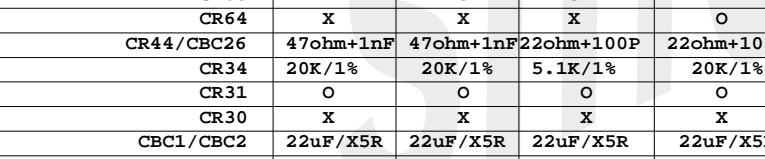
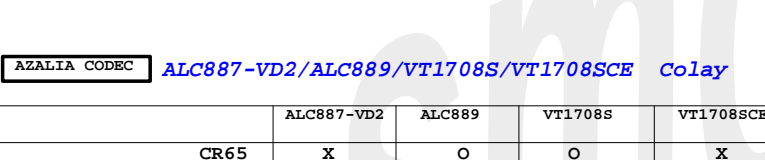
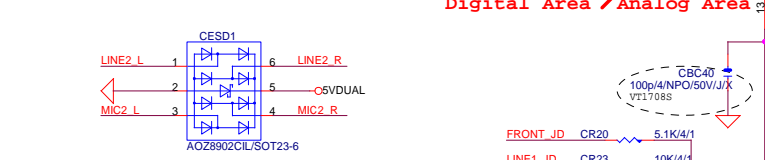
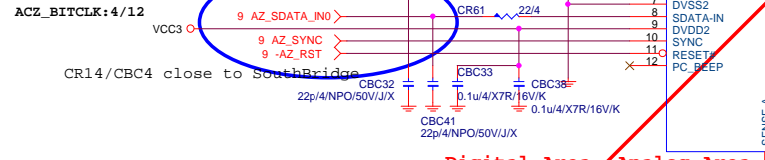
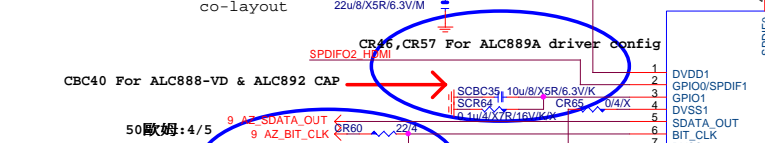
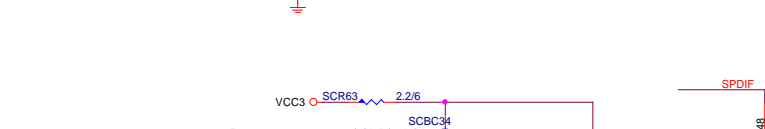
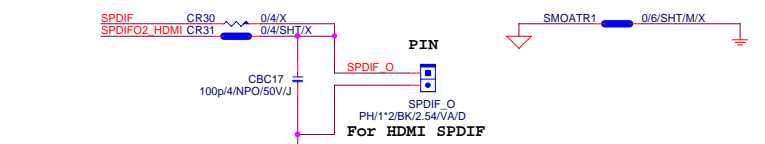
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Hardware Monitor circuits



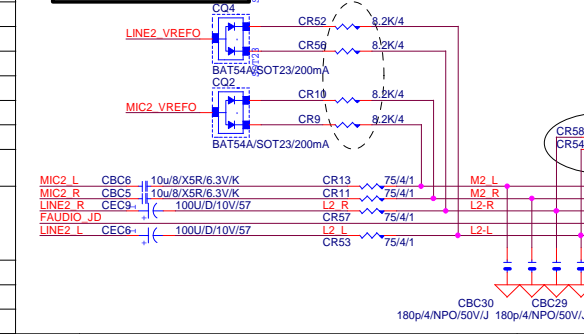
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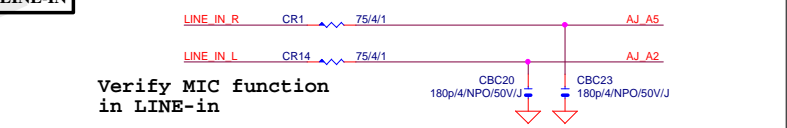
AZALIA CODEC ALC887-VD2/ALC889/VT1708S/VT1708SCE Colay

	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	O	O	X
CR64	X	X	X	O
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR34	20K/1%	20K/1%	5.1K/1%	20K/1%
CR31	O	O	O	O
CR30	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CBC35	O	X	X	O
CBC39/CBC40	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR13/CR11/CR57/CR53	75 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	O	X	X	O
CD2/CD3/CQ3/CQ5	X	O	O	X
CR1/CR14/CR17/CR22	75 ohm	62 ohm	1K ohm	1K ohm

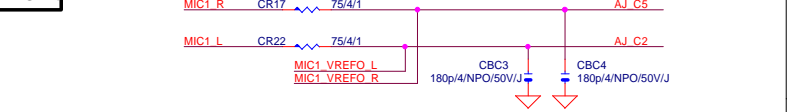
AZALIA FRONT PANEL



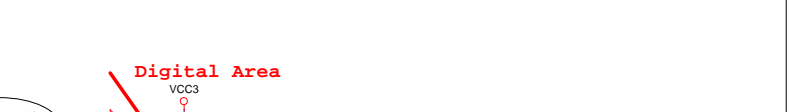
LINE-IN



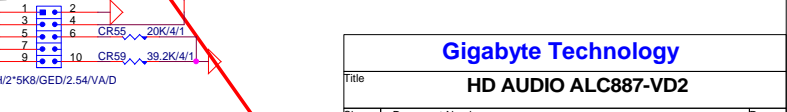
MIC-IN



LINE-OUT



LINE-OUT

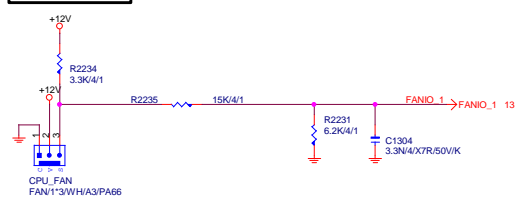


LINE-OUT

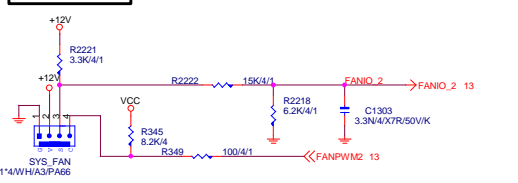


Gigabyte Technology			
HD AUDIO ALC887-VD2			
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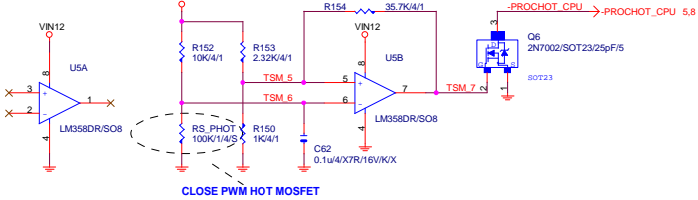
CPU FAN



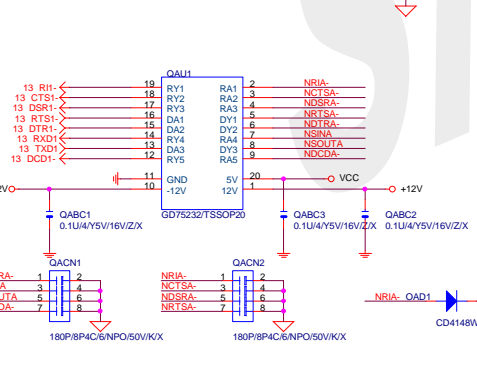
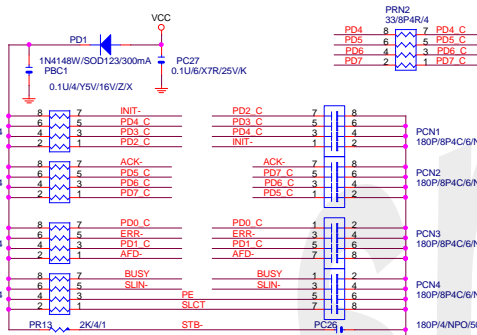
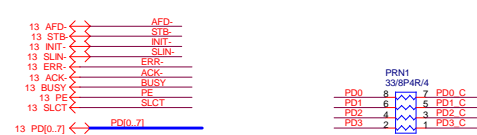
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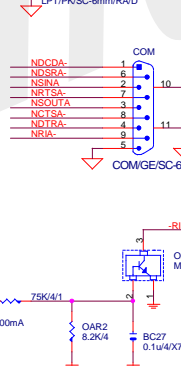
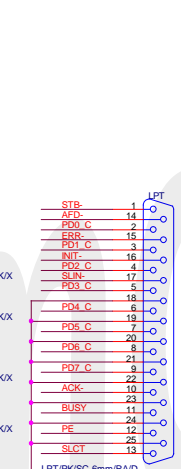
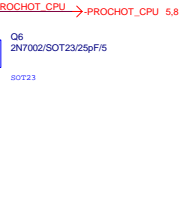
RS_PHOT CLOSE CPU VR MOSFET



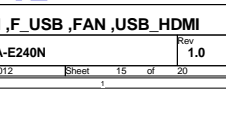
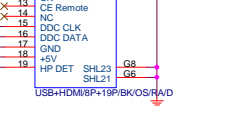
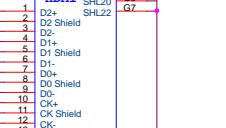
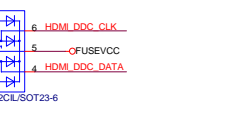
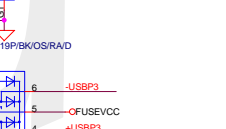
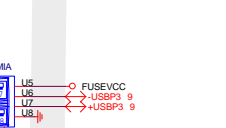
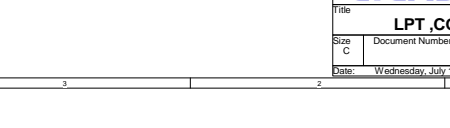
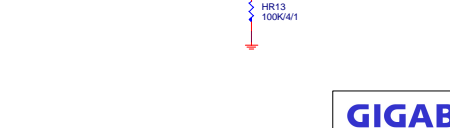
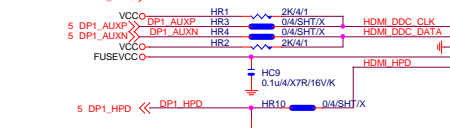
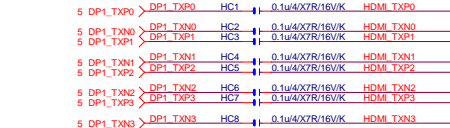
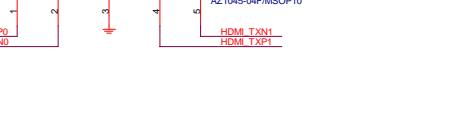
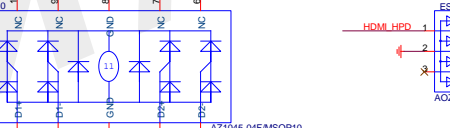
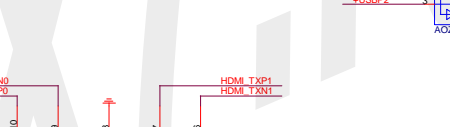
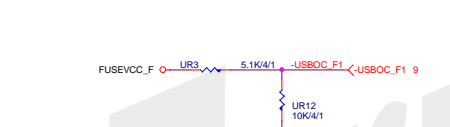
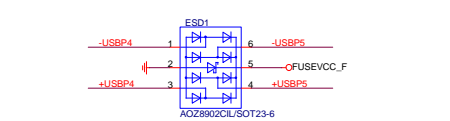
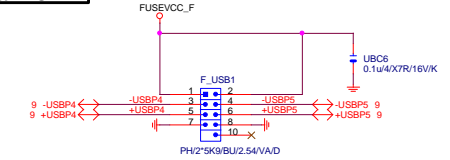
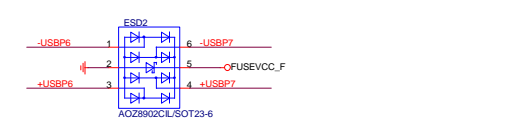
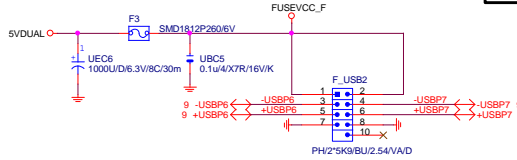
CLOSE PWM HOT MOSFET



Deasserted at 116 degree

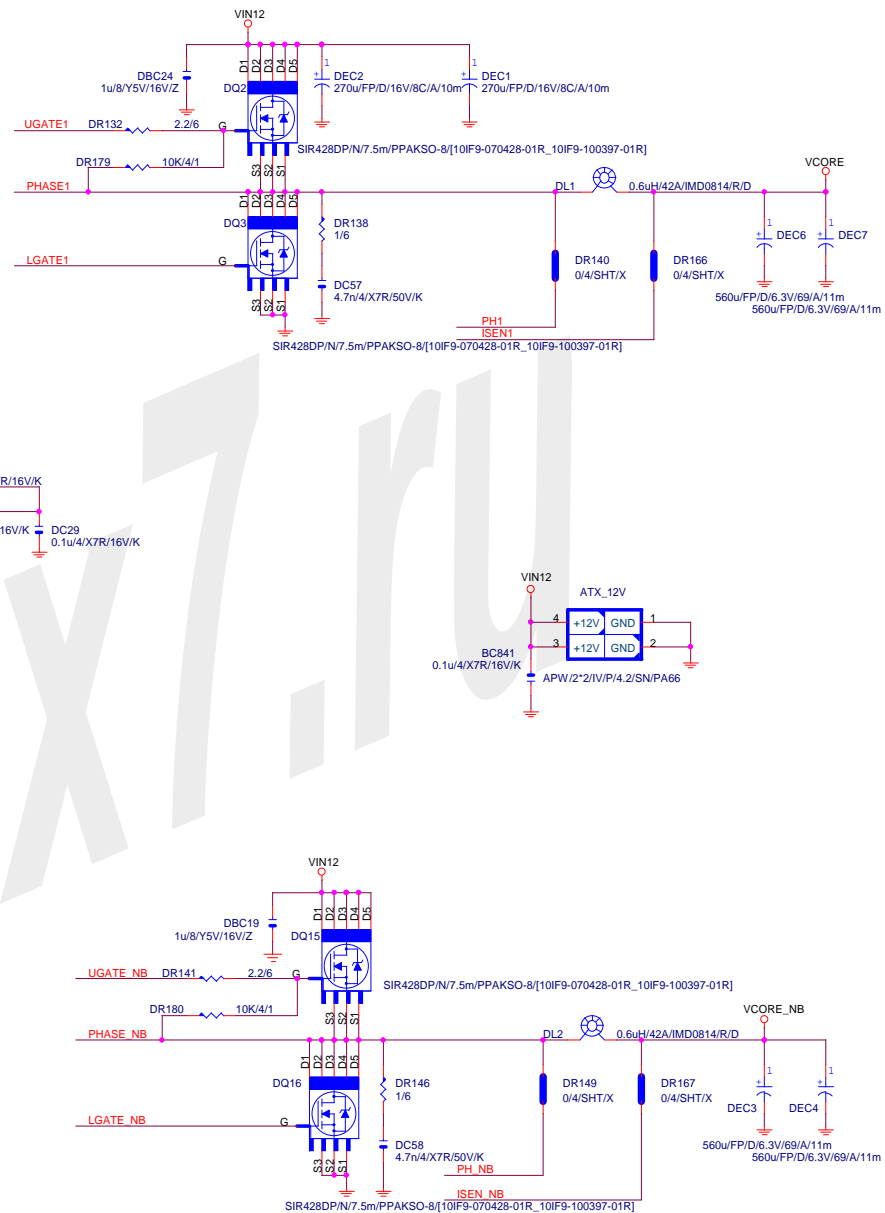
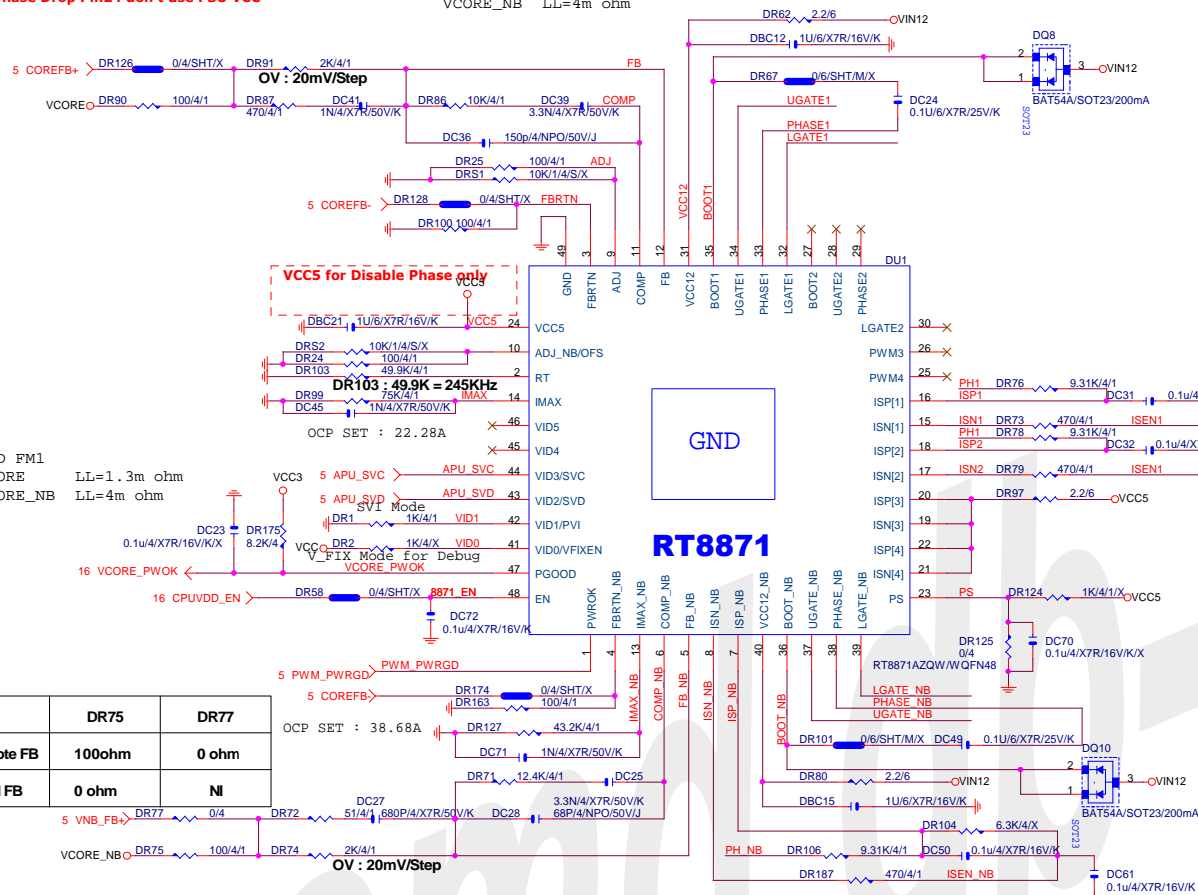


FRONT USB



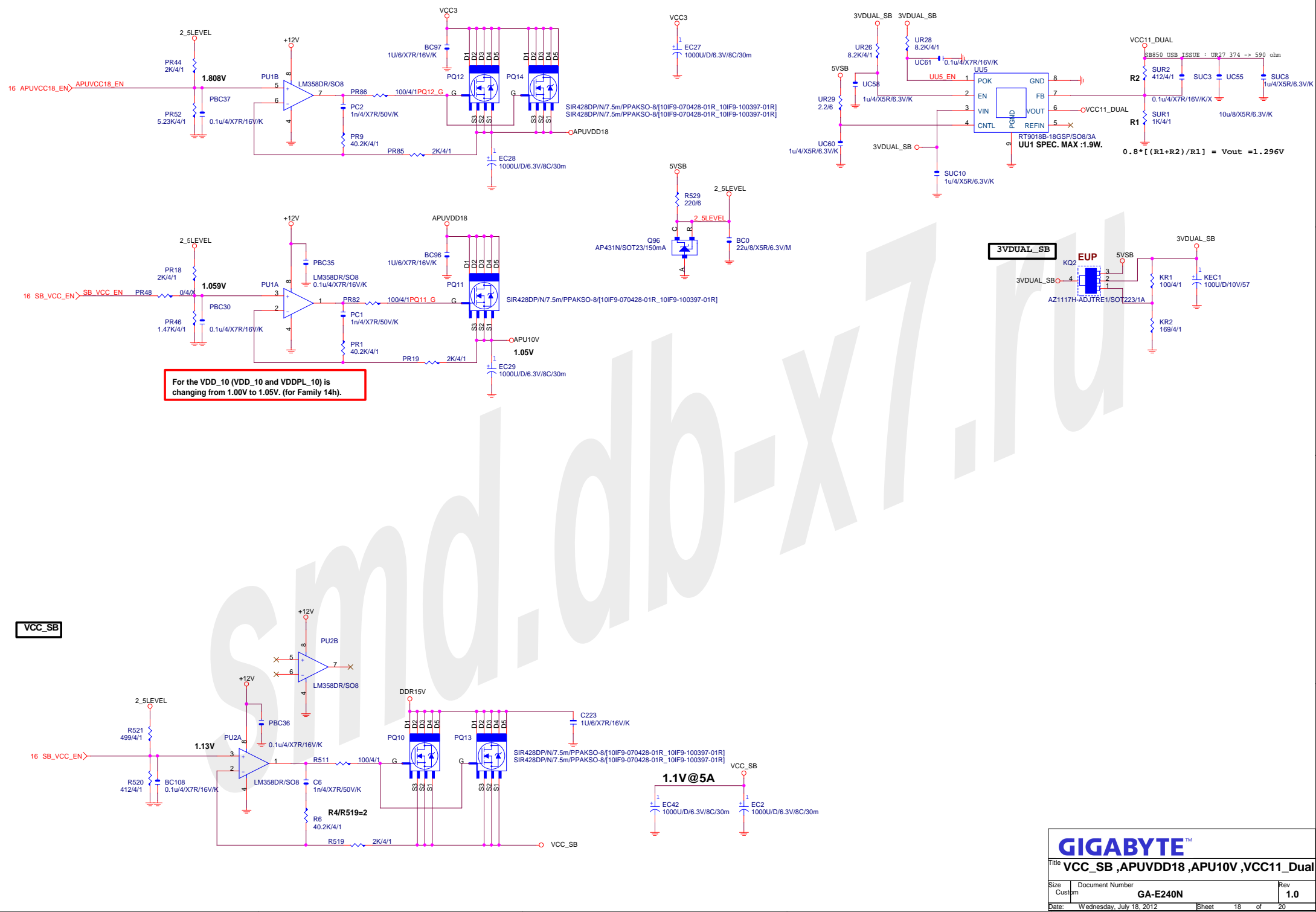
Note :
Phase disable pull Hi, Connect to Pin 24 VCC5,
Phase Drop Pin24 don't use PSU VCC

AMD FM1
VCORE LL=1.3m ohm
VCORE_NB LL=4m ohm



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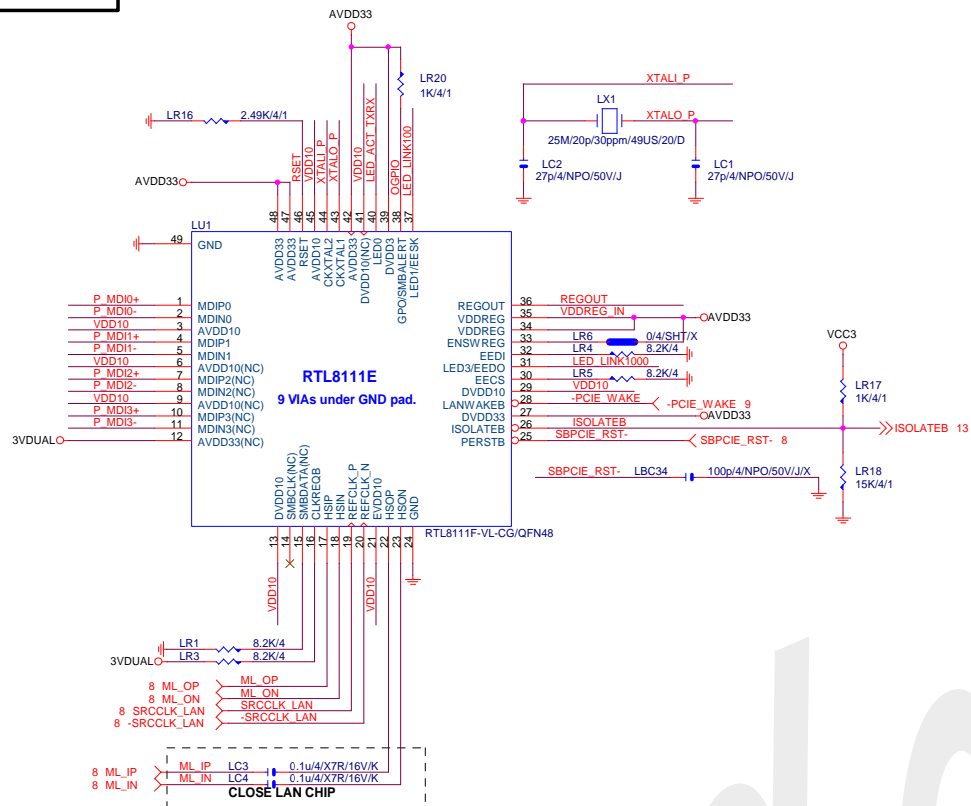
Title			PWM RT8871	
Size	Document Number	GA-E240N		Rev
Custm				1.0
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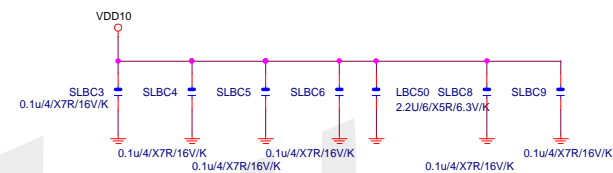
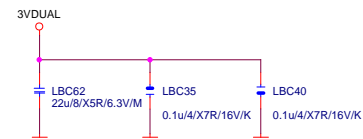
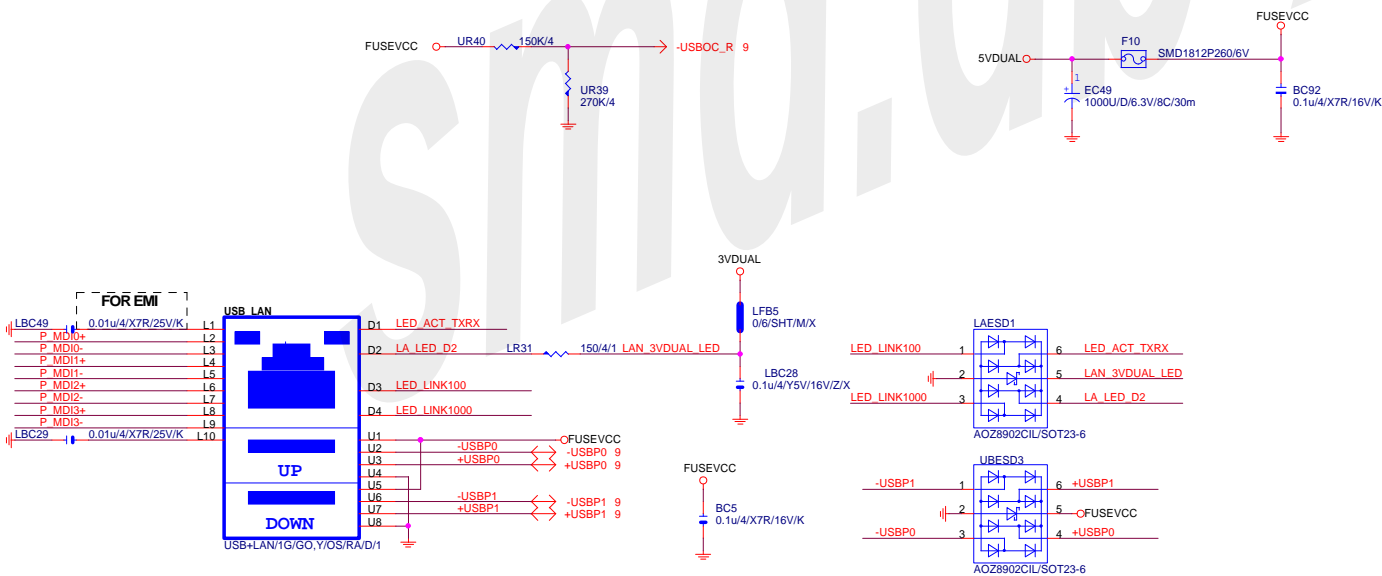
For the VDD_10 (VDD_10 and VDDPL_10) is changing from 1.00V to 1.05V. (for Family 14h).

$$0.8 * [(R1+R2)/R1] = V_{out} = 1.296V$$

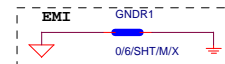
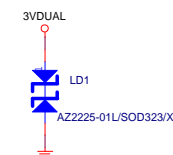
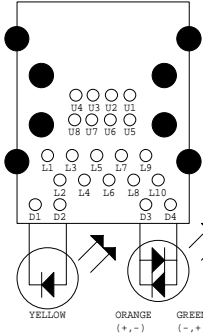
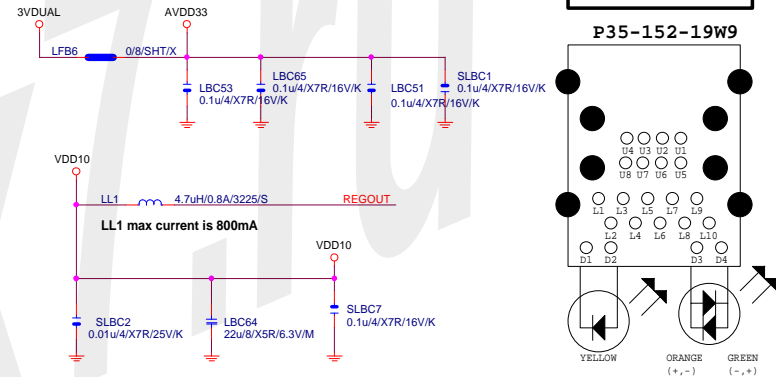
PCIE-1G LAN



USB_LAN



USB_LAN CONNECTOR



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